

Figure 1 is a schematic diagram of a system 10. The system includes a grid-like structure 200, which is bounded by a curved line 204. A series of arrows 201, 203, 205, and 210 indicate a path or flow. A dashed line 220 is also shown. A small inset 202 is located in the upper right corner.

FIG. 2



FIG. 3a



FIG. 3b

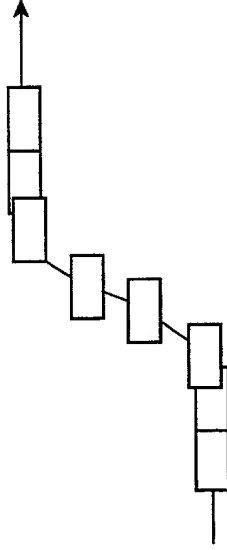
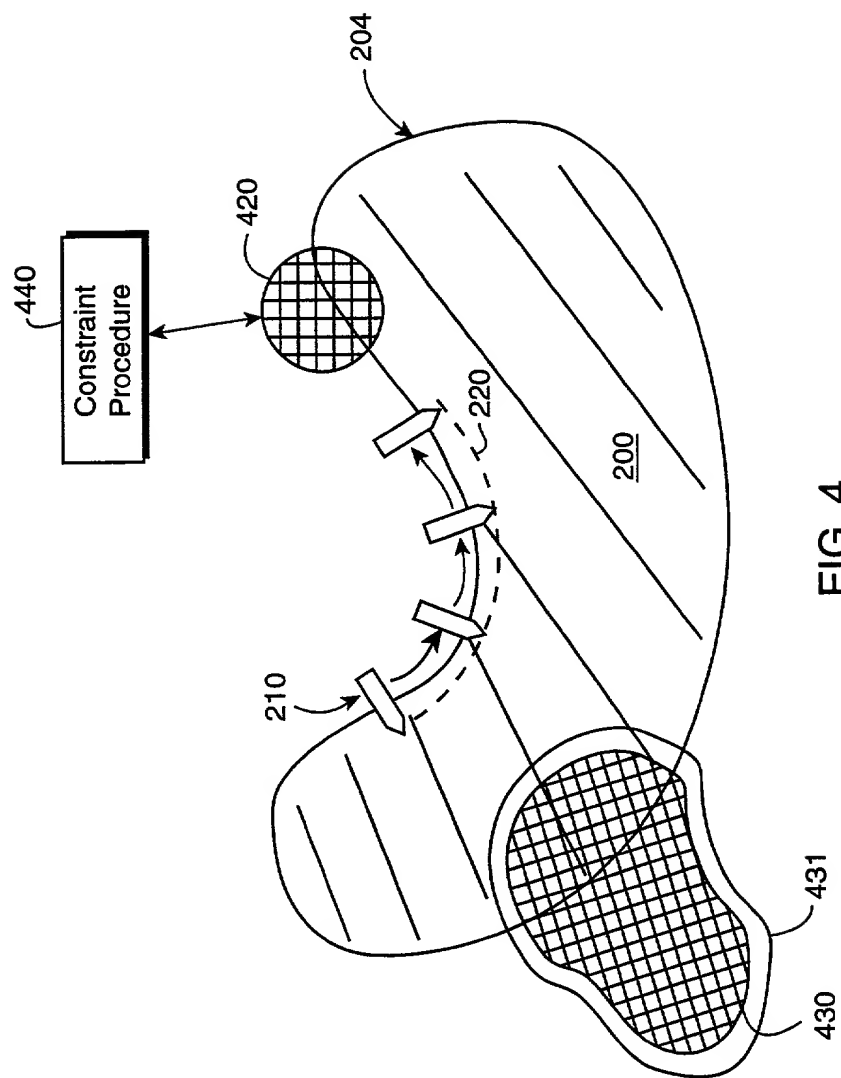


FIG. 3c



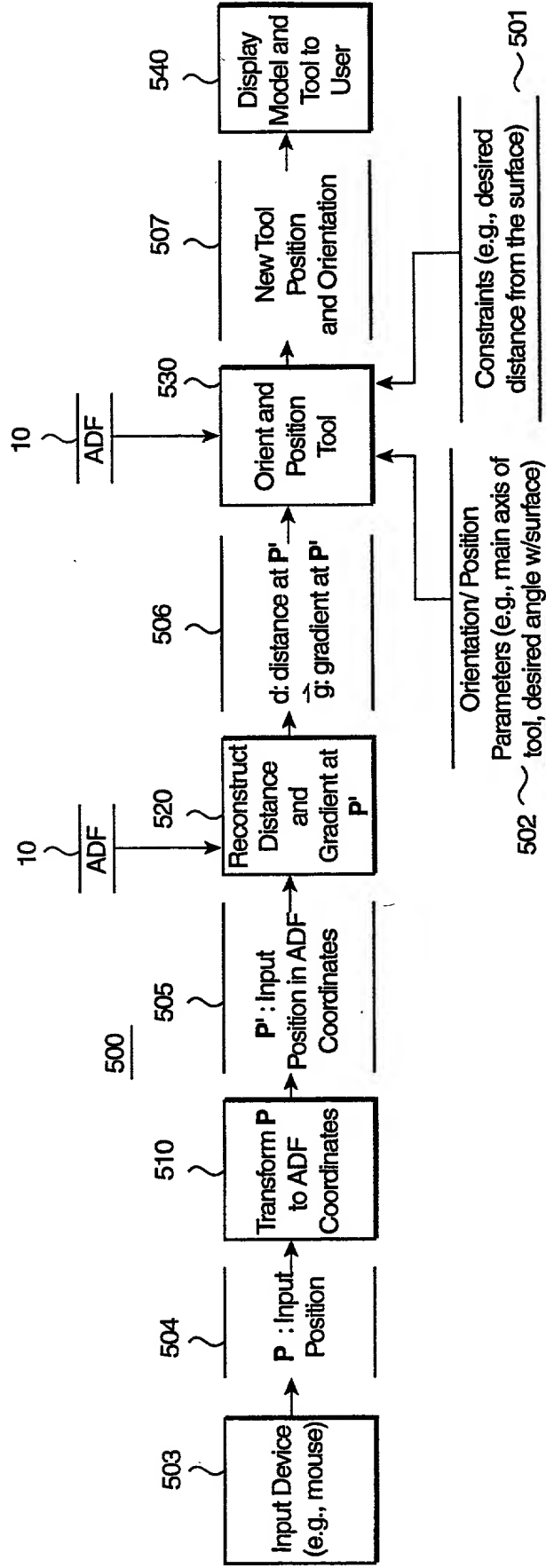
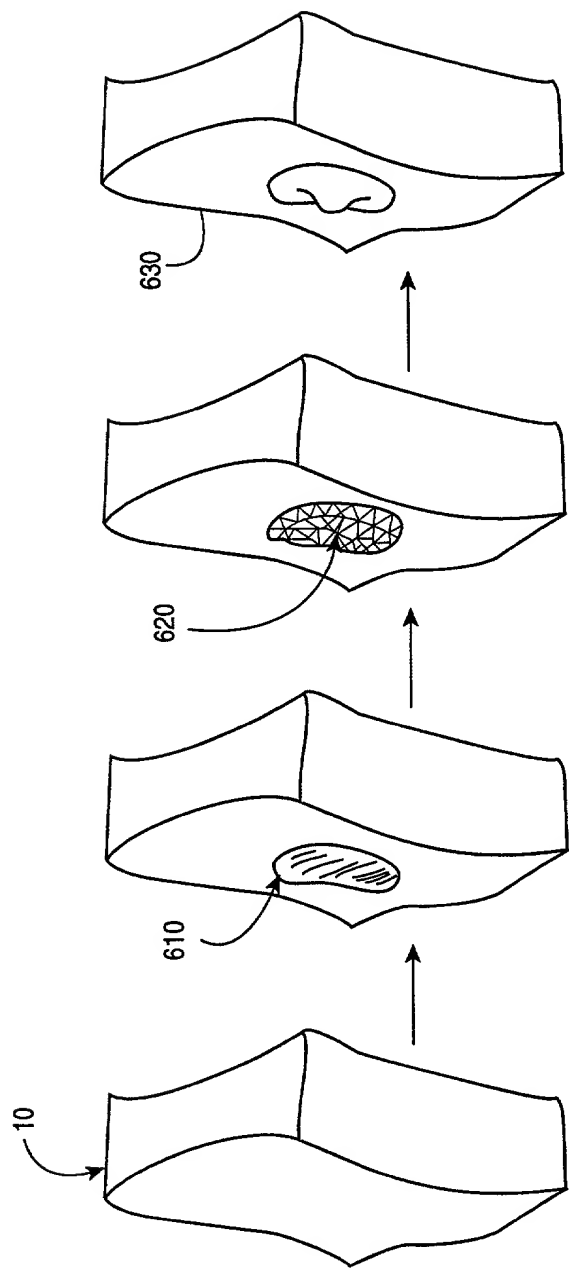


FIG. 5

FIG. 6



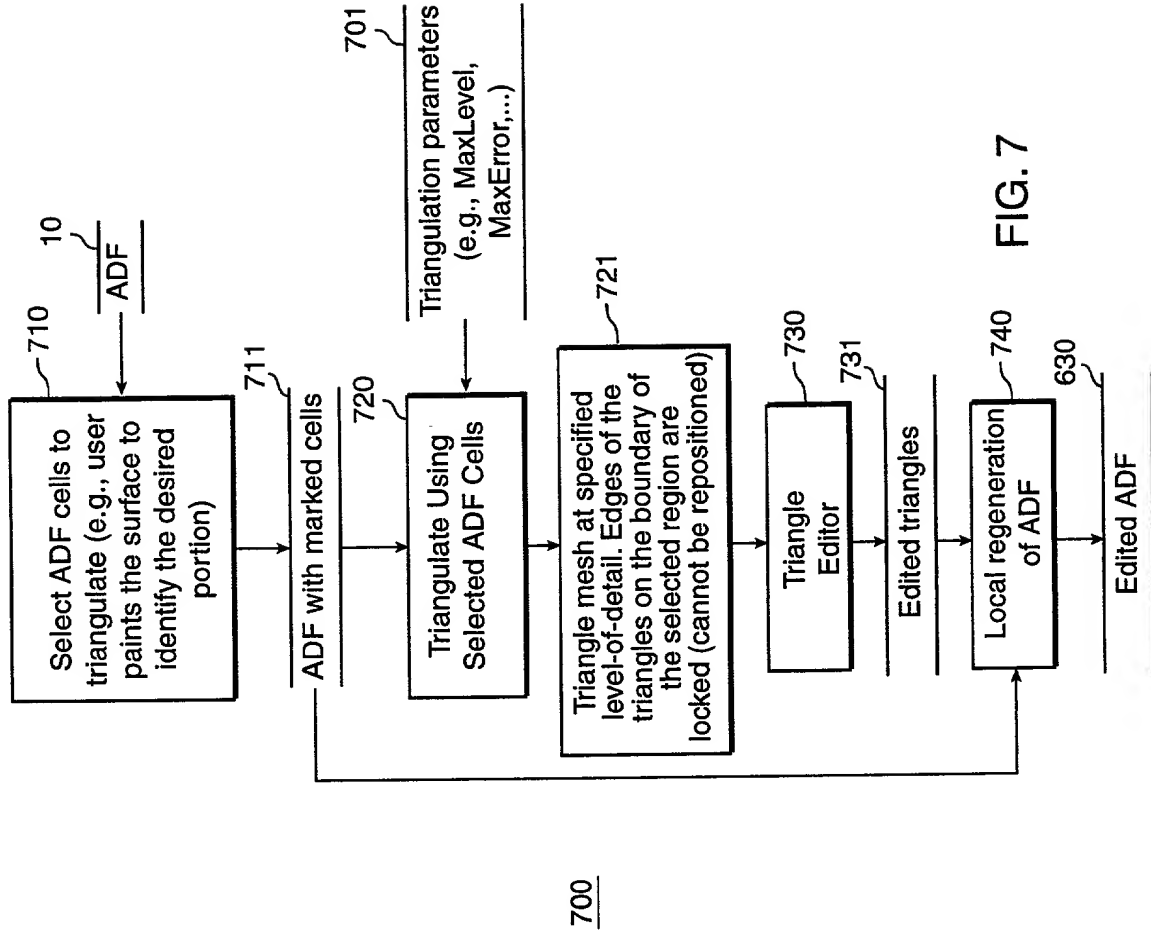


FIG. 7

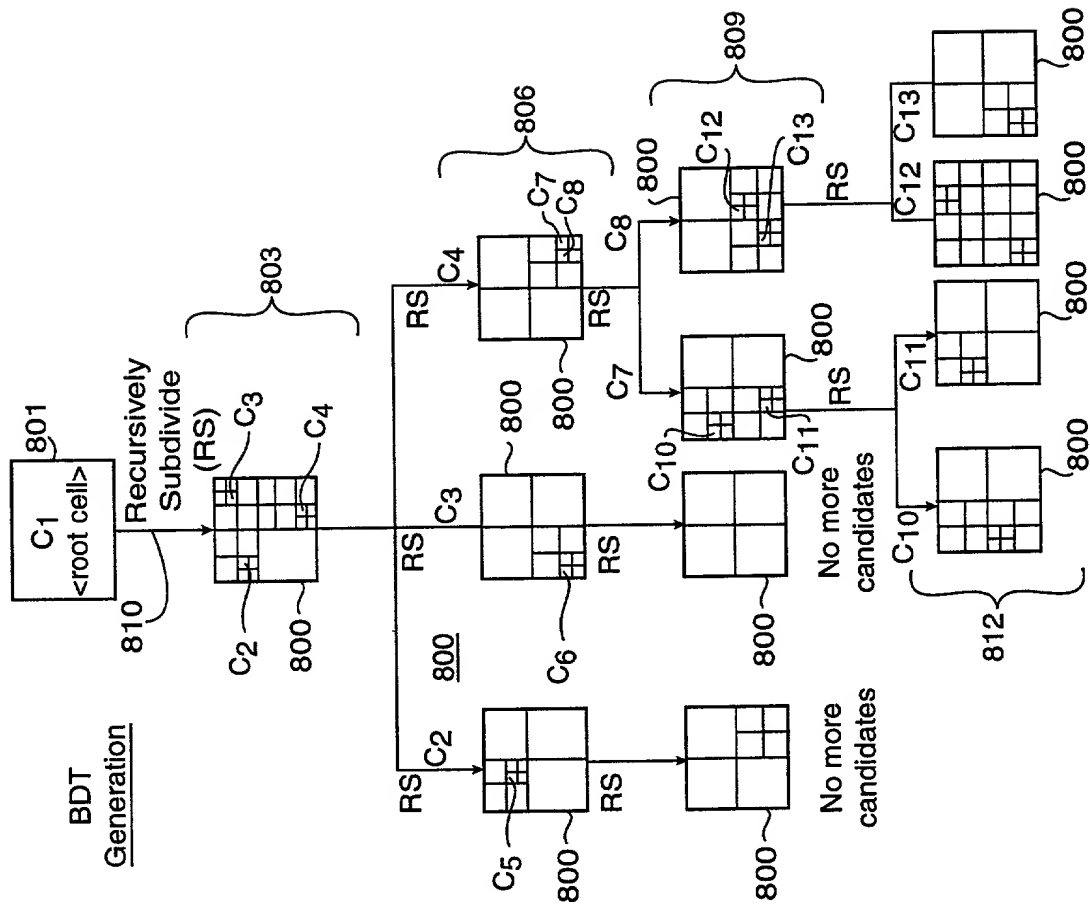


FIG. 8



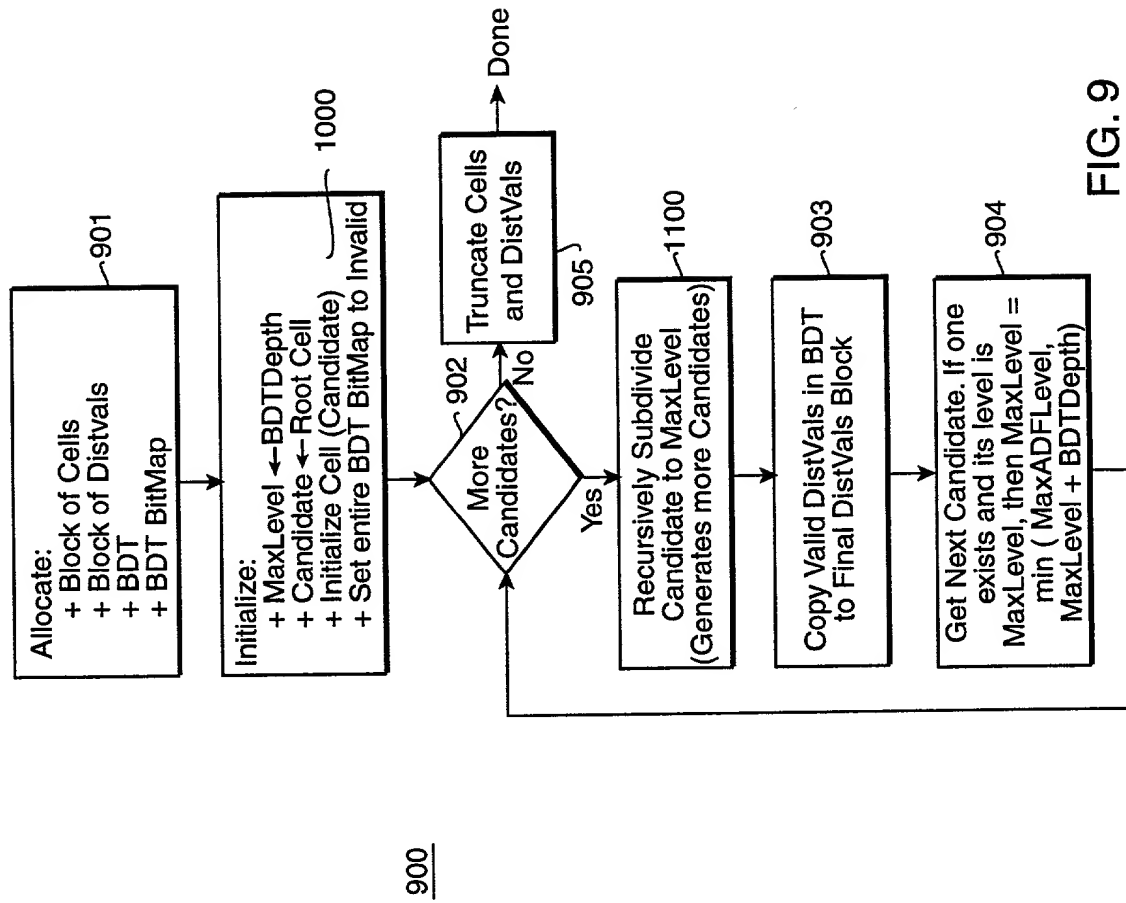


FIG. 9

FIG. 10 is a block diagram of a system 1000 for computing cell error. The system 1000 includes a block 1001 for initializing cell fields (e.g., parent, bounding box, level, ...), a block 1009 for computing cell error using BDT to avoid redundant distance computations, and a block 1000 for setting cell error. The block 1001 outputs to the block 1009, which also receives inputs from the BDT 133 and the BDT Bitmap 1009. The block 1009 outputs to the block 1000.

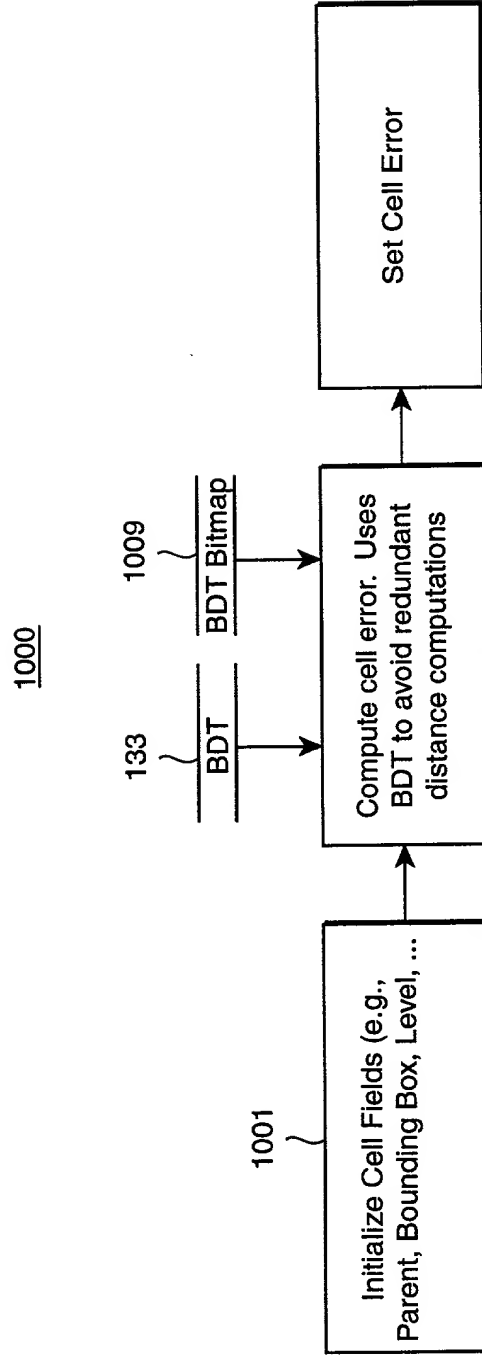


FIG. 10

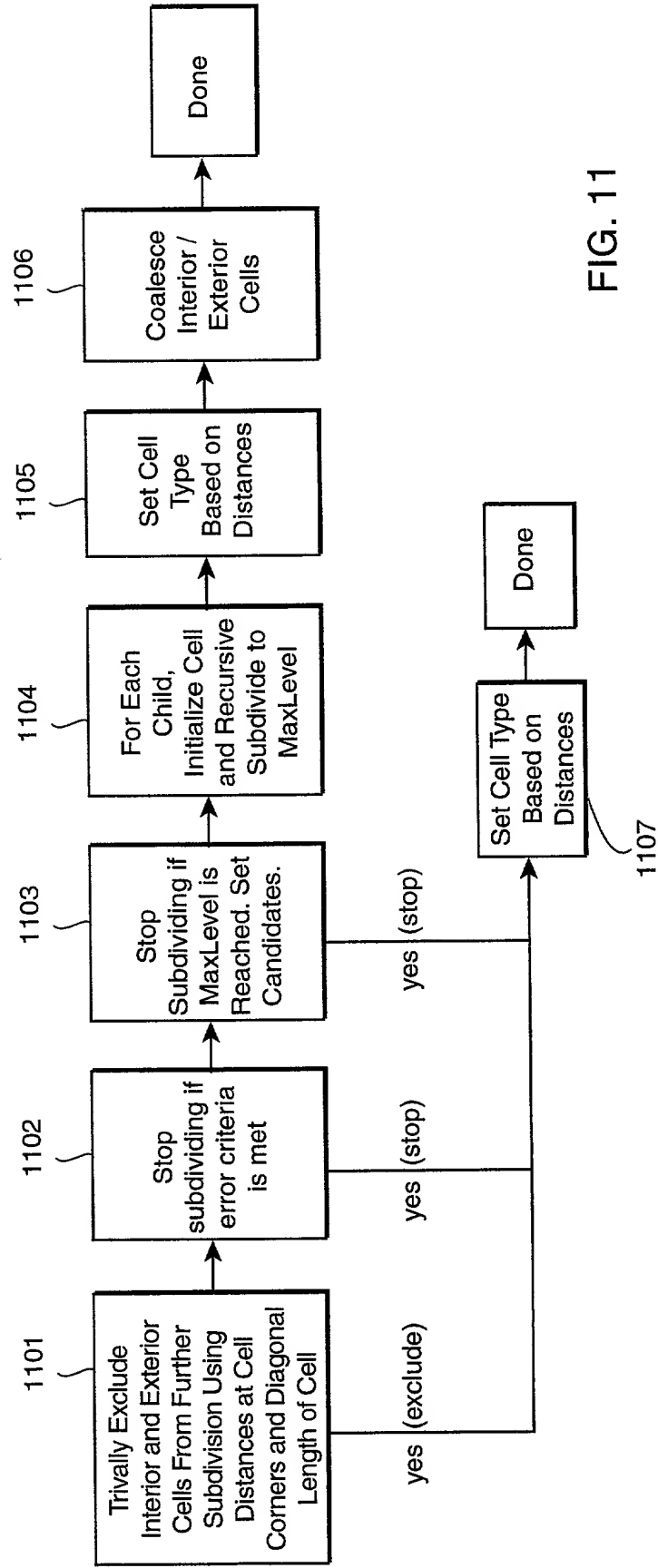


FIG. 11

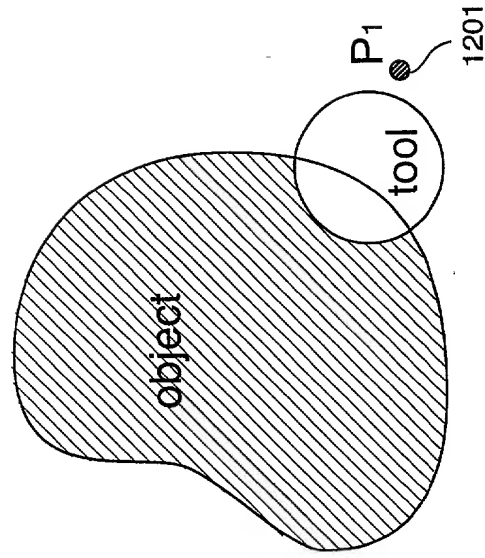


FIG. 12a

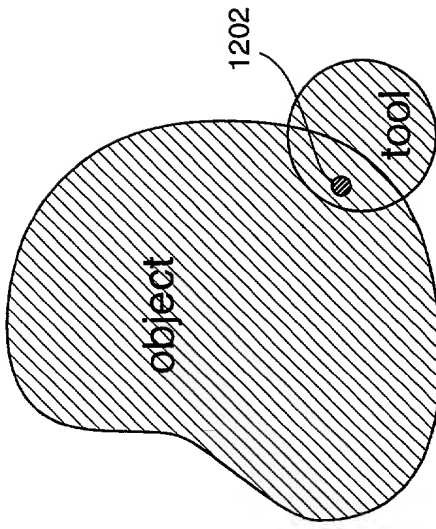


FIG. 12b

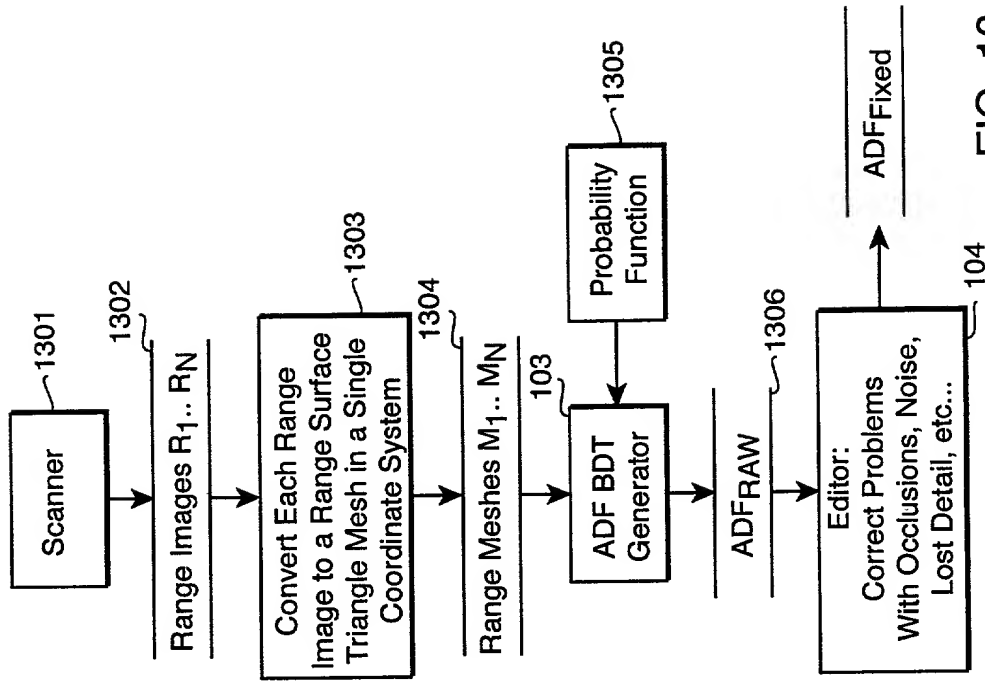
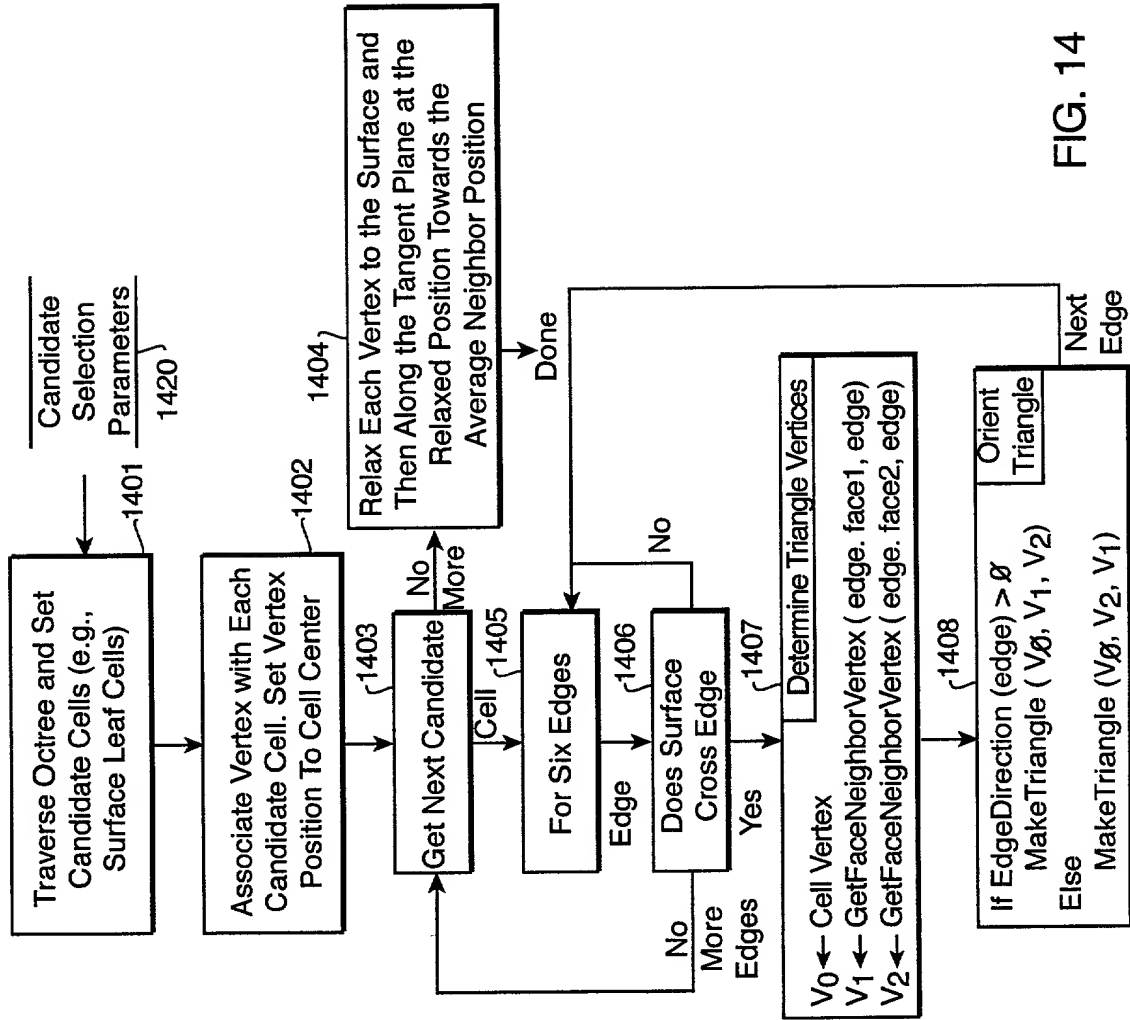


FIG. 13



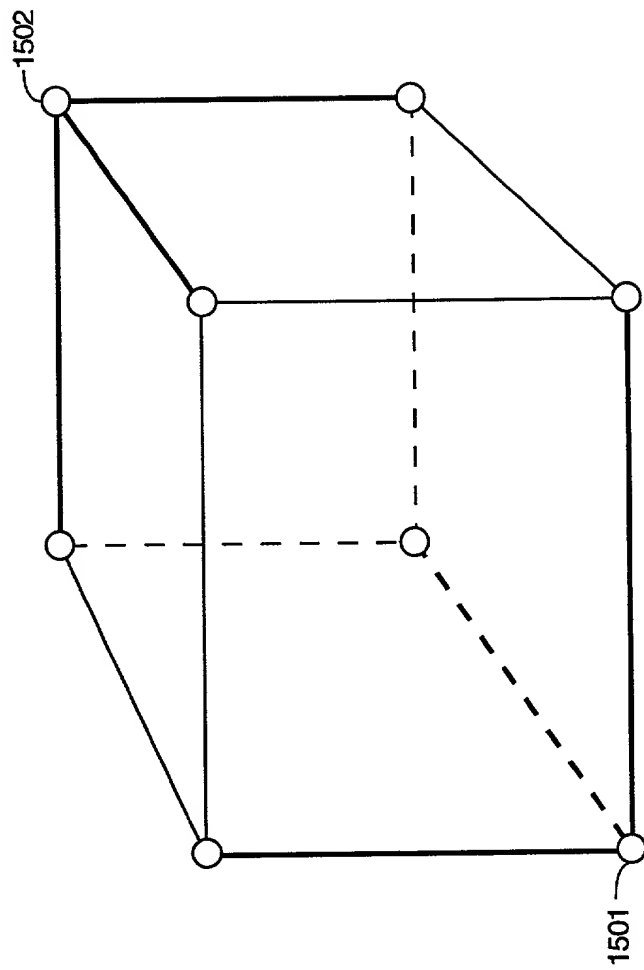


FIG. 15

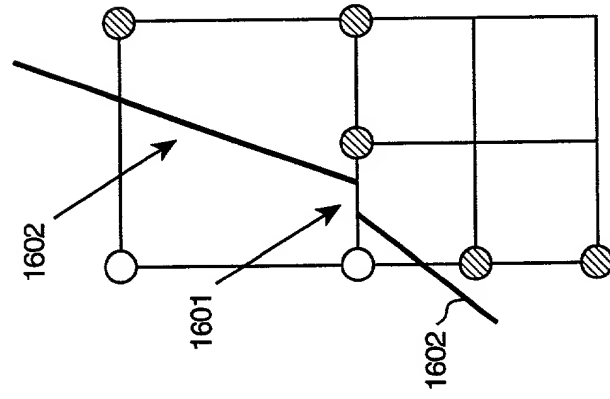


FIG. 16a

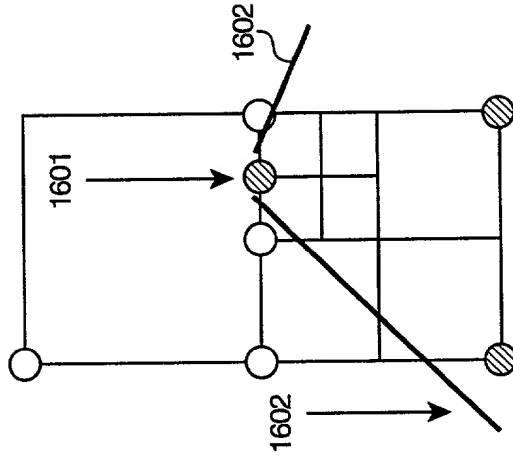


FIG. 16b



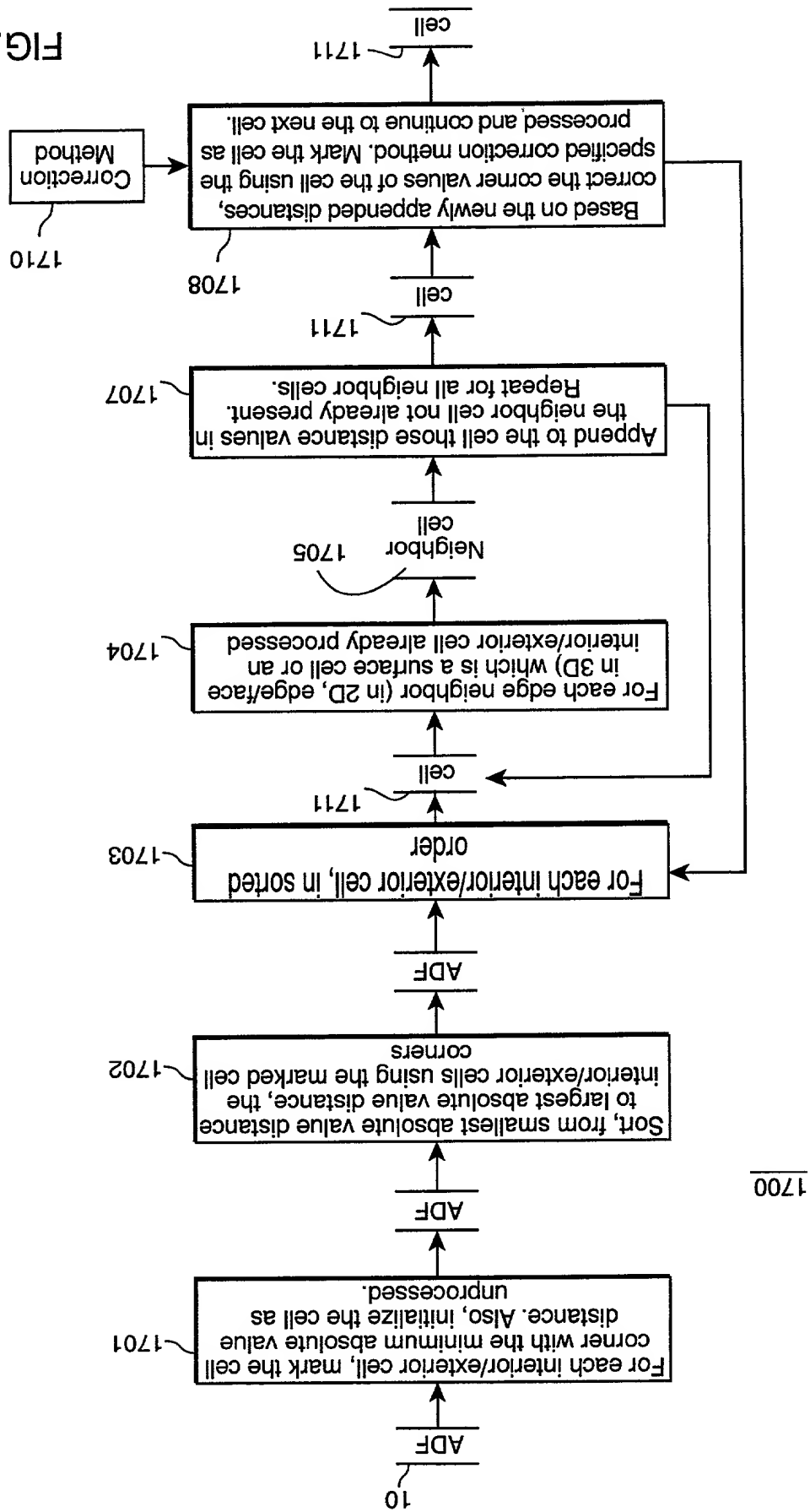


FIG. 17